/\*

u8g\_dev\_ssd1309\_128x64.c

Universal 8bit Graphics Library

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\*/

#include "u8g.h"

#define WIDTH 128

#define HEIGHT 64

#define PAGE\_HEIGHT 8

/\* ssd1309 ini sequence\*/

static const uint8\_t u8g\_dev\_ssd1309\_128x64\_init\_seq[] PROGMEM={

U8G\_ESC\_CS(0), /\* disable chip \*/

U8G\_ESC\_ADR(0), /\* instruction mode \*/

U8G\_ESC\_RST(1), /\* do reset low pulse with (1\*16)+2 milliseconds \*/

U8G\_ESC\_CS(1), /\* enable chip \*/

0xfd,0x12, /\*Command Lock \*/

0xae, /\*Set Display Off \*/

0xd5,0xa0, /\*set Display Clock Divide Ratio/Oscillator Frequency \*/

0xa8,0x3f, /\*Set Multiplex Ratio \*/

0x3d,0x00, /\*Set Display Offset\*/

0x40, /\*Set Display Start Line\*/

0xa1, /\*Set Segment Re-Map\*/

0xc8, /\*Set COM Output Scan Direction\*/

0xda,0x12, /\*Set COM Pins Hardware Configuration\*/

0x81,0xdf, /\*Set Current Control \*/

0xd9,0x82, /\*Set Pre-Charge Period \*/

0xdb,0x34, /\*Set VCOMH Deselect Level \*/

0xa4, /\*Set Entire Display On/Off \*/

0xa6, /\*Set Normal/Inverse Display\*/

U8G\_ESC\_VCC(1), /\*Power up VCC & Stabilized \*/

U8G\_ESC\_DLY(50),

0xaf, /\*Set Display On \*/

U8G\_ESC\_DLY(50),

U8G\_ESC\_CS(0), /\* disable chip \*/

U8G\_ESC\_END /\* end of sequence \*/

};

/\* select one init sequence here \*/

#define u8g\_dev\_ssd1309\_128x64\_init\_seq u8g\_dev\_ssd1309\_128x64\_init\_seq

static const uint8\_t u8g\_dev\_ssd1309\_128x64\_data\_start[] PROGMEM = {

U8G\_ESC\_ADR(0), /\* instruction mode \*/

U8G\_ESC\_CS(1), /\* enable chip \*/

0x010, /\* set upper 4 bit of the col adr to 0 \*/

0x000, /\* set lower 4 bit of the col adr to 4 \*/

U8G\_ESC\_END /\* end of sequence \*/

};

static const uint8\_t u8g\_dev\_ssd13xx\_sleep\_on[] PROGMEM = {

U8G\_ESC\_ADR(0), /\* instruction mode \*/

U8G\_ESC\_CS(1), /\* enable chip \*/

0x0ae, /\* display off \*/

U8G\_ESC\_CS(0), /\* disable chip \*/

U8G\_ESC\_END /\* end of sequence \*/

};

static const uint8\_t u8g\_dev\_ssd13xx\_sleep\_off[] PROGMEM = {

U8G\_ESC\_ADR(0), /\* instruction mode \*/

U8G\_ESC\_CS(1), /\* enable chip \*/

0x0af, /\* display on \*/

U8G\_ESC\_DLY(50), /\* delay 50 ms \*/

U8G\_ESC\_CS(0), /\* disable chip \*/

U8G\_ESC\_END /\* end of sequence \*/

};

uint8\_t u8g\_dev\_ssd1309\_128x64\_fn(u8g\_t \*u8g, u8g\_dev\_t \*dev, uint8\_t msg, void \*arg)

{

switch(msg)

{

case U8G\_DEV\_MSG\_INIT:

u8g\_InitCom(u8g, dev, U8G\_SPI\_CLK\_CYCLE\_300NS);

u8g\_WriteEscSeqP(u8g, dev, u8g\_dev\_ssd1309\_128x64\_init\_seq);

break;

case U8G\_DEV\_MSG\_STOP:

break;

case U8G\_DEV\_MSG\_PAGE\_NEXT:

{

u8g\_pb\_t \*pb = (u8g\_pb\_t \*)(dev->dev\_mem);

u8g\_WriteEscSeqP(u8g, dev, u8g\_dev\_ssd1309\_128x64\_data\_start);

u8g\_WriteByte(u8g, dev, 0x0b0 | pb->p.page); /\* select current page (SSD1306) \*/

u8g\_SetAddress(u8g, dev, 1); /\* data mode \*/

if ( u8g\_pb\_WriteBuffer(pb, u8g, dev) == 0 )

return 0;

u8g\_SetChipSelect(u8g, dev, 0);

}

break;

case U8G\_DEV\_MSG\_CONTRAST:

u8g\_SetChipSelect(u8g, dev, 1);

u8g\_SetAddress(u8g, dev, 0); /\* instruction mode \*/

u8g\_WriteByte(u8g, dev, 0x081);

u8g\_WriteByte(u8g, dev, (\*(uint8\_t \*)arg) >> 2);

u8g\_SetChipSelect(u8g, dev, 0);

return 1;

case U8G\_DEV\_MSG\_SLEEP\_ON:

u8g\_WriteEscSeqP(u8g, dev, u8g\_dev\_ssd13xx\_sleep\_on);

return 1;

case U8G\_DEV\_MSG\_SLEEP\_OFF:

u8g\_WriteEscSeqP(u8g, dev, u8g\_dev\_ssd13xx\_sleep\_off);

return 1;

}

return u8g\_dev\_pb8v1\_base\_fn(u8g, dev, msg, arg);

}

U8G\_PB\_DEV(u8g\_dev\_ssd1309\_128x64\_hw\_spi, WIDTH, HEIGHT, PAGE\_HEIGHT, u8g\_dev\_ssd1309\_128x64\_fn, U8G\_COM\_HW\_SPI);

U8G\_PB\_DEV(u8g\_dev\_ssd1309\_128x64\_sw\_spi, WIDTH, HEIGHT, PAGE\_HEIGHT, u8g\_dev\_ssd1309\_128x64\_fn, U8G\_COM\_SW\_SPI);

U8G\_PB\_DEV(u8g\_dev\_ssd1309\_128x64\_i2c, WIDTH, HEIGHT, PAGE\_HEIGHT, u8g\_dev\_ssd1309\_128x64\_fn, U8G\_COM\_SSD\_I2C);